DREZNO

BINARY
CONVERSION
KOMPUTOR II

Model of 1989

OPERATOR'S MANUAL *rev. 1989/2.0*

SALUT

Thank you for purchasing this Xaoc Devices product. Drezno II ['drɛznɔ] is a component of the Leibniz Binary Subsystem, a family of 8-bit signal processing devices offering comprehensive manipulation of signals and voltages in the digital domain. Drezno II is the input/output front-end of the system consisting of an analog-to-digital converter (ADC) and a digital-to-analog converter (DAC). In other words, it converts from continuous analog signals to a stream of digital numbers from 0 to 255 (the binary data) and from a stream of digital numbers to an analog signal. These numbers are transmitted using eight parallel binary (two-state, on/off) signals that may be gates, clocks, rhythms, etc. Even on its own, Drezno II can be used for waveshaping of analog signals and voltages based on their binary representation. The two halves of the module may be used entirely independently or linked through the data ribbon cable, possibly with other Leibniz modules installed between the ADC and the DAC.

Drezno II is an upgraded version of the original Drezno released in 2017. It uses new converters of much higher resolution, which results in a lower noise floor and higher accuracy down to the lowest bit. It can be used for quantizing pitch voltages. Potentiometer ranges are factory calibrated for the chromatic scale within 10Vpp (128 semitone steps) and 20Vpp (256 semitone steps).

To better understand the device and avoid common pitfalls, we strongly advise the user to read through the entire manual before using the module.

INSTALLATION

Drezno II requires 12hp worth of free space in the Eurorack cabinet. Always turn the power off before plugging the module into the bus board using the supplied 16-wire ribbon cable, paying close attention to power cable pinout and orientation. The red stripe indicates the negative rail and should match the arrow head or **-12V** *mark on the bus board and the unit. Drezno II is internally secured against reversed power connection; however, flipping the 16-pin header* **MAY CAUSE SERIOUS DAMAGE** *to other components of your system because it will short-circuit the +12V and +5V power lines.*

Besides power, you need to pay attention to properly connect the Leibniz interface (fig. 1). For standalone operation (using Drezno II without any additional Leibniz modules), bridge the **OUT** *and* **IN** *headers with the supplied 10-wire ribbon data cable. For expanding your Leibniz setup, use the additional cables included with your other modules in the subsystem. The general rule is to connect the* **OUT** *header of Drezno II to the* **IN** *header of some other module that will receive the ADC data (e.g., Rostock, Poczdam, Jena) and to connect the* **OUT** *header of some other module that provides data (e.g., Ostankino, Erfurt, Jena, etc.) to the* **IN** *header of Drezno II.* **AVOID PLUGGING OUT TO OUT.** *Observe the arrowhead or dot indicating the red stripe orien-*

Binary numbers are like common decimal numbers, except they don't use 10 different digits (from 0 to 9) but just two (0 and 1), called bits. For example, 203 in the decimal system means "two times a hundred plus a three," while 101 in the binary system means "one times a four plus a one." Why four? Because in a 3-digit binary (base-2) number, the digits represent 2^2=4, 2^1=2, and 2^0=1, just like in the 3-digit decimal (base-10) number they represent 10^2=100, 10^1=10, and 10^0=1.

*Note that in both cases, the exponents correspond to the position of the digit. The first digit/bit in a notation is the most significant in both decimal and binary systems because it informs the amount of the strongest component of the sum, while the last digit/bit is the least significant. For example, in an 8-bit system, the highest bit represents 2^7=128, and the lowest bit represents 2^0=1. Since there are eight bits, and each can have only two values, there are 2*2*2*2*2*2*2*2 = 2^8=256 combinations possible, from 0 (code 00000000) to 255 (code 11111111).*

The significance of bits is vital because it indicates how sensitive a number is to changing a single digit. Thus, manipulating individual bits may have a huge impact on the value (when bit 7 is affected) or be barely noticeable (when bit 0 is affected), and vice versa: small changes in signal amplitude often affect only the lower bits, while the highest bits react mostly to big changes.

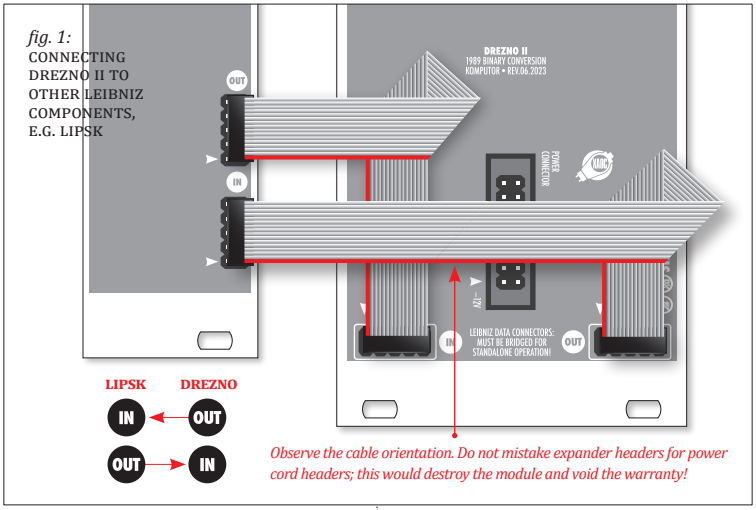


fig. 1: CONNECTING DREZNO II TO OTHER LEIBNIZ COMPONENTS, E.G. LIPSK

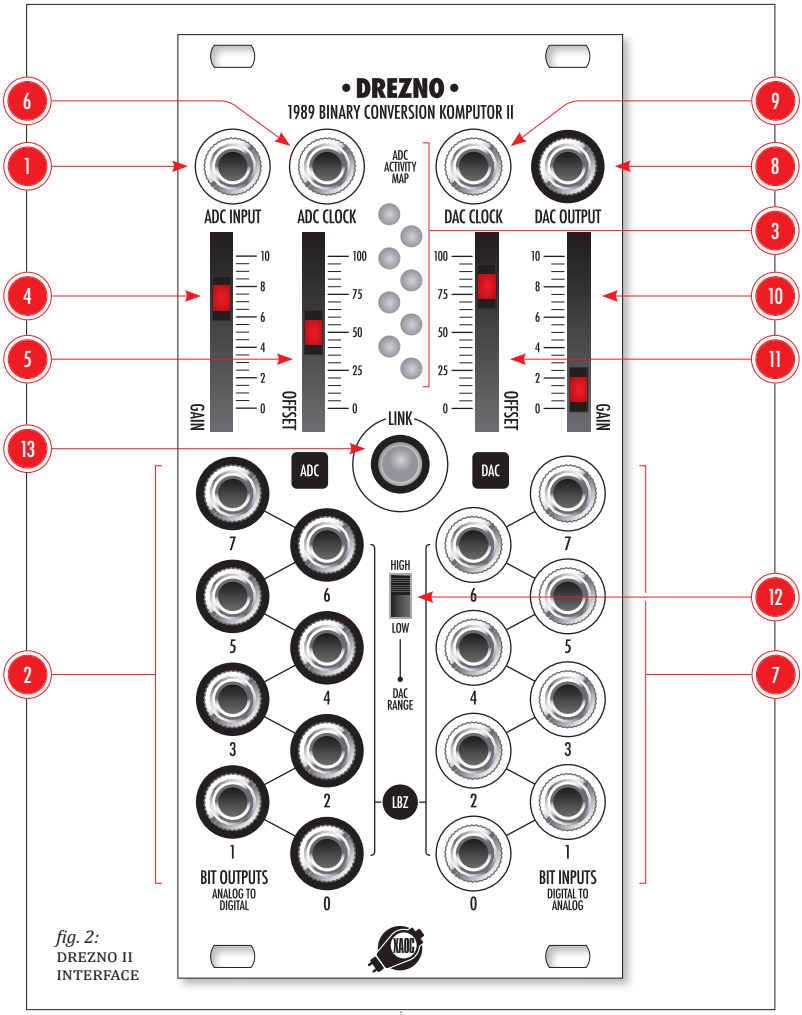


fig. 2:
DREZNO II
INTERFACE

tation on the Leibniz header of each module (not always pointing in the same direction). Incorrectly plugged cables will result in entirely erroneous operation.

WARNING: NEVER PLUG POWER INTO THE 10-PIN LEIBNIZ DATA HEADERS, *as this would heavily damage your Drezno II and jeopardize other modules connected to it.*

The module should be fastened by mounting the supplied screws before powering up.

MODULE OVERVIEW

Drezno II (fig. 2) consists of two sections that can work independently or as a linked pair. The **ADC INPUT** ❶ *accepts CV and audio signals. There are eight A/D* **BIT OUTPUTS** ❷*, representing each of the eight bits (7 down to 0) with a 5V gate signal. In addition,* **BIT OUTPUTS'** *activity is indicated by the corresponding set of eight yellow* **ADC ACTIVITY MAP** *LEDs* ❸*.*

The illuminated **GAIN** ❹ *and* **OFFSET** ❺ *sliders allow you to adapt the range of the input analog signal to the A/D converter's dynamic range. The sliders' bi-color LEDs indicate signal amplitude (***GAIN***), clipping (***OFFSET***), and polarity (both). The colors are used according to industrial standards: red represents positive, and green represents negative values. The converter chip expects only positive voltages, so for bipolar input signals, set the* **OFFSET** *slider in the upper position, which will add some voltage to shift everything above 0V. With* **GAIN** *set to max, a 10Vpp input signal will fit the entire range, while a hotter signal might need to be attenuated (depending on the desired result).*

The A/D converter is clocked internally at a very high rate (near 2MHz), which helps to avoid aliasing for audio rate signals, but it also means the binary output signals may change at extreme rates. The **ADC CLOCK** *input* ❻ *allows you to override the internal clock with your own clock, which is necessary when you want to slow down the rate both at the front panel jacks and in the Leibniz data output. It accepts gate, trigger, and clock signals, and reacts to the rising edge.*

The DAC section mirrors the ADC section. There are eight D/A **BIT INPUTS** ❼*, accepting 5V gate signals representing each of the bits numbered from 7 to 0. The* **DAC OUTPUT** ❽ *produces a CV or audio signal based on the input code. The* **DAC CLOCK** *input* ❾ *expects gate/trigger signals and is normalled to the clock delivered via the ribbon cable connected to the Leibniz* **IN** *data socket at the back of the module. Therefore, even though the DAC clock by default follows the ADC clock, it can be replaced by a clock produced by any Leibniz module, and it can be overridden by any signal patched through the panel socket.*

The DAC section also features **GAIN** ❿ *and* **OFFSET** ⓫ *sliders which set the level and shift of the* **DAC OUTPUT** *signal. Similarly, their bi-color LEDs indicate the amplitude and polarity of the output signal (***GAIN***) and warn against possible clipping at the output stage*

*(**OFFSET**). To achieve a bipolar output signal, set the **OFFSET** slider to a lower position, subtracting some voltage from the positive-only output of the D/A converter and making it swing around 0V.*

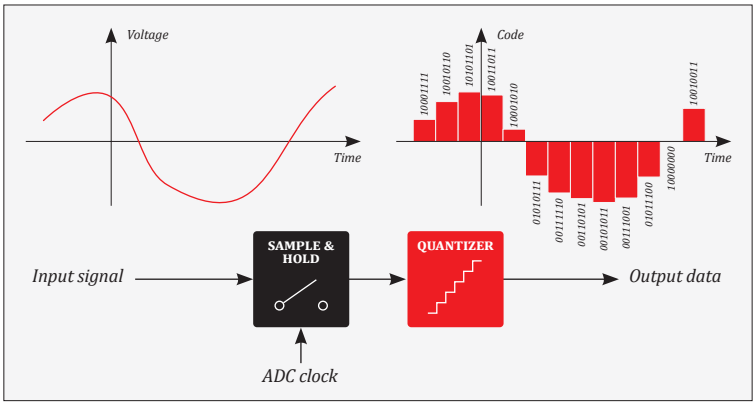
*The D/A converter is calibrated and offers precise 1/12V steps when the **GAIN** slider is at maximum. A range of 256 semitones is equivalent to over 20 octaves or over 20Vpp, which may sometimes be impractical. The **DAC RANGE** miniature switch ⓬ selects between this full range and a narrower 10+ octave range (128 semitones) by ignoring the lowest significant bit and scaling everything down by 1/2.*

*The illuminated **LINK** button ⓭ connects the data arriving at the Leibniz **IN** header at the back as normalization signals for the **BIT INPUTS.** Patching any cable into any DAC binary input breaks its normalization and overrides it with the external signal. However, with no signals patched to the inputs, the converter receives either the bits from the Leibniz data cable (when **LINK** is engaged) or just 00000000 (when **LINK** is off). This arrangement allows you to replace only a few bits from the incoming data or disconnect the DAC from the Leibniz source entirely and use only the front panel jacks.*

THE PRINCIPLE OF OPERATION

The ADC section of Drezno II converts analog signals to digital numbers. This process consists of sampling the voltage at each clock cycle followed by quantization of the sampled value (fig. 3). During quantization, the value is compared to a set of discrete levels, which are numbered from 0 to 255. For example, if

fig. 3: THE PRINCIPLE OF A/D CONVERSION



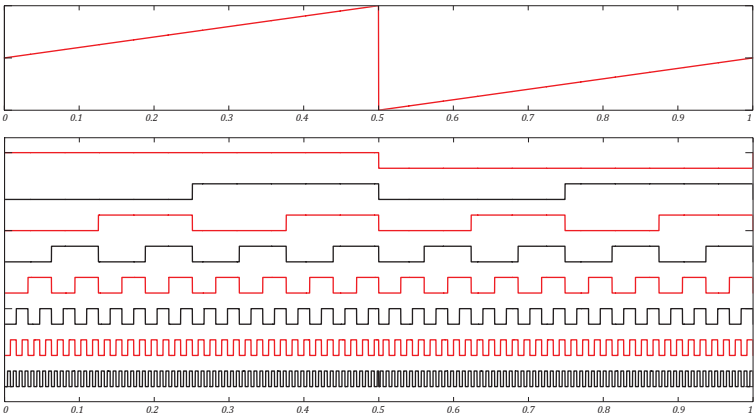
the converter is scaled to the -5V to 5V range, and 0V is being quantized, it falls exactly at the middle of the scale, resulting in 128. The number is expressed using eight bits of binary code. For example, 128 is represented as 10000000. In other words, bit 7 is set to 1, and the remaining bits are 0.

*The physical representation of these bits is eight parallel gate signals (binary 0=0V, binary 1=5V). In our example, 5V is at the highest bit output (***BIT 7***), and 0V is at all the lower outputs. The same signals are delivered to the pins of the Leibniz* **OUT** *header at the back of the module and transmitted alongside the clock to other modules through the Leibniz data ribbon cable. It is possible to connect a chain of multiple Leibniz modules connected in series or even build a complex system with data splits and loops.*

Feeding a time-varying signal to the ADC input of Drezno II results in the **BIT OUTPUTS** *changing in response (fig. 4 and 5). At each instant, their combined state represents the corresponding value of the input signal at that time. For example, observe that when the analog wave reaches its maximum, all bit values are 1. Note that the most significant bit changes the slowest since it only shows whether the signal is above or below the middle of the range, while the lowest bits may change very quickly.*

Please keep in mind that there is always some noise in every analog part of the circuit; hence the input signal is not perfectly clean. That means the transitions between binary 0's and 1's may not be singular, especially with a high-frequency clock. We recommend using a slower ADC clock when you need more stable

fig. 4: INPUT SAWTOOTH SIGNAL AND RESULTING INDIVIDUAL BIT SIGNALS



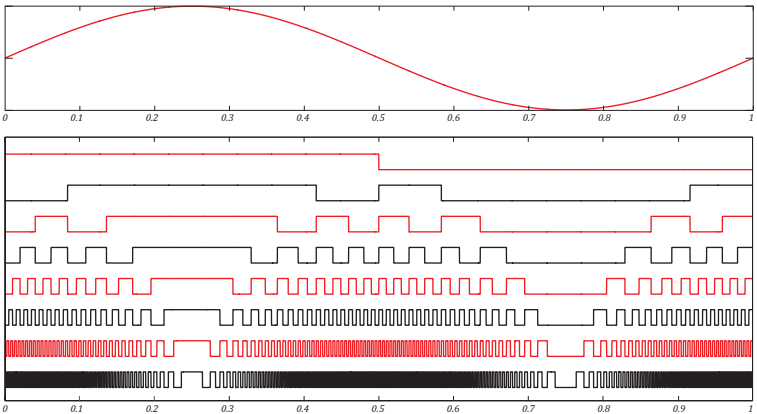
gates or triggers from the **BIT OUTPUTS** *or want a slow stream of data.*

The DAC section of Drezno II converts digital numbers to voltages. It features a clock-driven data latch that holds the recent combination of bits during conversion. The clock for the D/A converter is supplied from the **DAC CLOCK** *input at the front panel, which in turn is normalled to the clock received from the Leibniz* **IN** *header. This may be the same as the* **ADC CLOCK** *when it is not modified or substituted in other Leibniz modules.*

The data fed to the converter is sourced directly from the front panel **BIT INPUTS**. *Each individual signal is one bit of the 8-bit code, and their combined state determines the input number (as described in the "Binary Code" infobox). For example, if there is an active 5V gate at input* **7** *and 0V at all the remaining inputs, the code is 10000000, which means 128 in the decimal system. This is the middle number of the 0...255 range of numbers and thus will be converted to the middle voltage of the current range of output voltages (determined by the* **DAC RANGE** *switch and the* **DAC OFFSET** *and* **GAIN** *sliders).*

The **BIT INPUTS** *jacks are optionally normalled to the signals received from the Leibniz* **IN** *header at the back of the module (provided* **LINK** *is active). Please note the D/A converter will not produce any analog signal if there is no Leibniz cable connected and no signals are patched into the jacks. Also, note that the output value is not updated until a new clock impulse occurs after the change of bits.*

fig. 5: INPUT SINUSOIDAL SIGNAL AND RESULTING INDIVIDUAL BIT SIGNALS



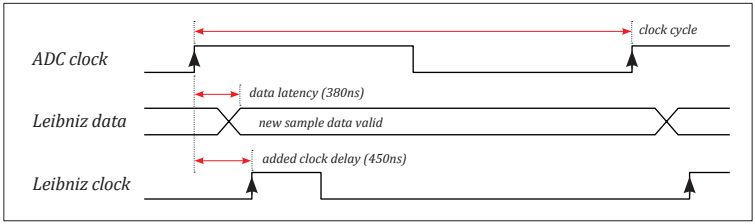


fig. 6: DELAYING OF ADC CLOCK TO ACOMMODATE THE TIME NEEDED FOR A/D CONVERSION

THE CONVERSION CLOCKS AND TIMING

Clocks are essential in digital systems. They synchronize the data flow because, at each cycle, the old value is passed to the next stage of a chain of devices, and a new value is taken from the preceding stage. All the logic or arithmetic processing inside digital circuits occurs between the edges of the clock signal. If the frequency is too high, it may cause data loss, processing errors, and glitches. On the other hand, a pipeline of processing stages yields some inevitable latency.

The internal clock of Drezno II is nearly 2MHz, which helps handle wideband signals without aliasing while minimizing latency. It is used as the sampling clock of the A/D converter, and it is also fed to the Leibniz **OUT** *header; hence any subsequent Leibniz module may operate synchronously with this clock. It can be replaced by any external clock signal (or even some irregular pattern of triggers or gates) patched to the* **ADC CLOCK** *input. Consider that each rising edge of the clock signal spawns a new process of sampling and then converting the sampled signal value, which both take some time (about 380ns). Therefore, the digital code resulting from this conversion is not instantly available. For this reason, Drezno II delays the clock's rising edge by about 450ns (to account for conversion time + propagation) before sending it to the Leibniz bus (fig. 6). Thanks to this little trick, the subsequent device (or Drezno II's DAC section) receives the code representing the most recent sample without waiting for the next clock cycle. It makes a significant difference when an external slow clock is patched to the* **ADC CLOCK** *input.*

Please keep in mind that the above solution only compensates for the conversion latency. It will not magically help if your clock's rising edge arrives after the change of input signal.

VOLTAGE RANGES, GAINS, AND OFFSETS

The input sensitivity and output voltage range of Drezno II are adjustable with **GAIN** *and* **OFFSET** *sliders. Note that the calibrated scales are only valid when these potentiometers are set at the extreme positions. With the ADC* **GAIN** *set to max, the input range is optimized for 10Vpp. For example, with* **OFFSET** *additionally set to min (for unipolar signals), an input*

CV=0V generates a binary code 00000000, CV=5V yields 10000000, and CV=+10V generates 11111111. Similarly, when **OFFSET** *is set to max (for bipolar signals), an input CV=-5V generates a binary code 00000000, CV=0V yields 10000000, and CV=+5V generates 11111111. If your signal is hotter, it will cause clipping in the A/D converter unless attenuated. In general, clipping is not dangerous, but will not yield correct binary code. Use clipping indicators in the* **OFFSET** *slider as a guide for optimum range settings.*

The DAC section has two range options selected with the slider switch. When set to **HIGH,** *it can generate voltages exceeding 20Vpp. With DAC* **GAIN** *set to max, a single change of the least significant bit corresponds to 1/12V (one semitone in the V/oct scale). Since there are 255 steps, the voltage range is 21.25Vpp. This is only possible if negative voltages are allowed. For example, setting the* **OFFSET** *slider to minimum yields 0V at the output when the input code is 10000000, -10.67V for 00000000, and +10.58V when the code is 11111111. There is nothing wrong with clipping when it is used intentionally. For example, setting the* **OFFSET** *slider to max yields 0V for the input code of 00000000 and 10.58V for input code 10000000. Higher binary numbers theoretically yield voltages that cannot be handled in Eurorack; hence they are clipped. The LED in the* **OFFSET** *slider shaft is lit whenever the range of -10V to +10V is exceeded. When the switch is set to* **LOW,** *the DAC section halves its output range, and the least significant bit is ignored. In other words, a 1/12V step corresponds to the input binary number changing by 2. There are 127 such steps, and the voltage range is thus 10.58Vpp which may be bipolar or unipolar. For example, setting the* **OFFSET** *slider to minimum produces 0V at the output with the input code 1000000x, 0000000x yields -5.33V, and 1111111x yields 5.25V. Setting the* **OFFSET** *slider to max produces unipolar voltages: 0V for code 0000000x, +5.33V for 1000000x, and +10.58V for 1111111x. The obvious application of these calibrated ranges is to produce pitch voltages. However, this is not the only use of the DAC section.*

When generating audio signals with Drezno II, you may need a lower amplitude but full resolution (no ignored bits). In such a case, set **DAC RANGE** *to* **HIGH,** *and DAC* **GAIN** *to a moderate value. It may then be necessary to adjust the* **OFFSET** *slider for bipolar output.*

PATCH EXAMPLES

• *When used standalone (with a loop cable installed at the back), processing of signals and voltages through ADC+DAC of Drezno II causes only a subtle 8-bit quantization effect. Modifying the binary representation creates various discontinuities in the transfer function, depending on which bits are affected. Some radical deformations of a CV or audio signal are achieved by cross-patching individual* **BIT OUTPUTS** *and* **BIT INPUTS** *(fig. 7). Many interesting, complex signal waveforms can be obtained by applying this to control voltages from LFOs, envelope generators, and even sequencers.*

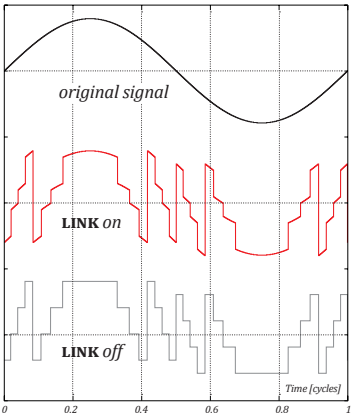


fig. 7: EXAMPLE WAVE DEFORMANTION RESULTING FROM CROSS-PATCHING BITS 7 AND 6, AND REPLACING BIT 6 WITH BIT 4

• Generating trigger patterns: feeding an LFO or any repeating CV into the ADC yields gate patterns (produced from the **BIT OUTPUTS***) that can be used for drum sequencing. Using a clock frequency pulse wave as the ADC clock allows for synchronizing the changes on individual outputs.*

• Generating melodies: the calibrated DAC section can produce V/oct voltages for driving a VCO. Use the same ADC input as above and set the ADC **GAIN** *low to constrain the pitch variations within a desired range. Substitute the DAC clock with gates from a sequencer or any other clock source for interesting variations.*

• Feeding the **BIT INPUTS** *with various combinations of gate signals (e.g., taken from binary counters like Xaoc Devices Erfurt, frequency dividers, or free-running oscillators) allows for synthesizing many interesting waveshapes or CV sequences at the DAC output.*

• Square wave folder/frequency multiplier: when a continuous waveform is fed into the ADC, individual binary outputs deliver pulse waveforms that flip between 0V and 5V many times per input period, depending on the level of details they represent. The average frequency of each individual input is twice as high as the frequency of the input above it, resulting in extremely fast waveforms at the least significant bit output. **NOTE:** *only input signals with linear slopes like a sawtooth or triangle yield uniform density signals at the binary outputs (compare figs 4 and 5).*

• Drezno II can be combined with other logic modules (like AND, OR, XOR, etc.), operating on individual bits or whole 8-bit numbers. In general, all low-level mathematical operations may be performed on signals and control voltages in this way.

CONNECTIVITY

Drezno II connects to all modules compatible with the Leibniz Binary Subsystem: Lipsk, Gera, Jena, Erfurt, Poczdam, Rostock, Ostankino II, and Odessa.

ACCESSORY

Our Coal Mine black panels are available for all Xaoc Devices modules. Sold separately. Ask your favorite retailer. •

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EASTERN BLOC TECHNOLOGIES

MADE IN THE EUROPEAN UNION

FEATURES

Universal analog-to-digital and digital-to-analog converter for processing analog signals in the 8-bit digital domain

Suitable for audio and CV processing with no aliasing

Component of the Leibniz Binary Subsystem

Accurate converters with calibrated voltage ranges

Independent ADC and DAC

SPECIFICATION

Eurorack synthesizer format compatible

12hp, 31mm deep (including the ribbon cable and bracket)

Current draw: +70mA/-40mA

Reverse power protection